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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,327	07/22/2003	Kyu-Mann Lee	5649-1136	7294

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,327	LEE ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10,13-29 and 34-38* is/are rejected.

7)☒ Claim(s) *8,9,11,12 and 30-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-38** are pending in the application is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in REPUBLIC OF KOREA, 10-2002-0044224 on 07/26/2002.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **1-7, 10, 13-29 and 34-38** are provisionally rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al., copending Application No. **10/136,991** which has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the copending application, it would constitute prior art under 35 U.S.C. 102(e), if published under 35 U.S.C. 122(b) or patented. This provisional rejection under 35 U.S.C. 102(e) is based upon a presumption of future publication or patenting of the copending application.

This provisional rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the copending application was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131. This rejection may not be overcome by the filing of a terminal disclaimer. See *In re Bartfeld*, 925 F.2d 1450, 17 USPQ2d 1885 (Fed. Cir. 1991).

Regarding claim **1**, Kim et al. disclose in Fig. 5 and the corresponding texts as set forth in paragraphs [0022]-[0030], a ferroelectric memory device comprises:

a semiconductor substrate (51);

a lower interlayer dielectric (74) on the semiconductor substrate;

a plurality of ferroelectric capacitors (82) on the lower interlayer dielectric; and

a plate line (87) that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors.

Regarding claim **2**, Kim et al. disclose in Fig. 5 the device further comprises:

an upper interlayer dielectric (89) on the lower interlayer dielectric and the plurality of ferroelectric capacitors; and

hydrogen barrier spacers (83a) between sidewalls of the ferroelectric capacitors and the lower interlayer dielectric.

Regarding claims **3 and 22**, Kim et al. disclose in Fig. 5 the device wherein the hydrogen barrier spacers are at least one from the group consisting of TiO_2, Al_2O_3, ZrO_2, and CeO_2 (see [0026]).

Regarding claim **4**, Kim et al. disclose in Fig. 5 the device wherein the plate line covers sidewalls of the hydrogen barrier spacers and a surface of the lower interlayer dielectric.

Regarding claim **5**, Kim et al. disclose in Fig. 5 the device wherein the plate line comprises:

a local plate line (87) directly contacting the surfaces of the at least two adjacent ferroelectric capacitors; and

a main plate line (97) on the upper interlayer dielectric opposite to the local plate line and directly contacting a surface of the local plate line via a slit-type via hole (95) through the upper interlayer dielectric.

Regarding claim **6**, Kim et al. disclose in Fig. 5 the device wherein the upper interlayer dielectric is between the local plate line and main plate line.

Regarding claim **7**, Kim et al. disclose in Fig. 5 the device wherein the plurality of ferroelectric capacitors are arranged in rows and columns.

Regarding claim **10**, Kim et al. disclose in Fig. 5 the device wherein the ferroelectric capacitor comprises a lower electrode (77), a ferroelectric pattern (79), and an upper electrode (81), wherein the plate line directly contacts the upper electrodes of at least two adjacent ones of the plurality of ferroelectric capacitors.

Regarding claim **13**, Kim et al. disclose the device wherein the ferroelectric pattern is at least one material from the group consisting of $SrTiO_3$, $BaTiO_3$, (Ba, Sr)TiO_3, Pb(Zr,Ti)O_3, $SrBi_2Ta_2O_9$, (Pb,La)(Zr,Ti)O_3, and $Bi_4Ti_3O_{12}$ ([0026]).

Regarding claim **14**, Kim et al. disclose the device wherein the plate line is at least one material from the group consisting of the platinum group including ruthenium, platinum, iridium, rhodium, Osmium, and palladium, and oxides thereof ([0027]).

Regarding claim **15**, Kim et al. disclose in Fig. 5 the device wherein the plate line is a local plate line directly contacting the surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, and further comprising an upper interlayer dielectric (89) covering the local plate line.

Regarding claim **16**, Kim et al. disclose in Fig. 5 the device further comprises an upper interlayer dielectric covering (89) on the plurality of ferroelectric capacitors, and wherein the plate line is a main plate line (97) directly contacting the surfaces of the at least two adjacent ones of the plurality of ferroelectric capacitors via a slit-type via hole (95) penetrating the upper interlayer dielectric.

Regarding claims **17-18**, Kim et al. disclose in Fig. 5 the device further comprises an insulation pattern (85a) between the plate line and the lower interlayer dielectric; and wherein the insulation pattern is an upper interlayer dielectric.

Regarding claim **19**, Kim et al. disclose in Fig. 5 the device further comprises an upper interlayer dielectric (89) on the plurality of ferroelectric capacitors, and main word lines (97) on the upper interlayer dielectric.

Regarding claim **20**, Kim et al. disclose in Fig. 5 and the corresponding texts as set forth in paragraphs [0022]-[0030], a method of fabricating a ferroelectric memory device, comprises:

forming a lower interlayer dielectric (74) on a semiconductor substrate (51);

forming a plurality of ferroelectric capacitors (82) on the lower interlayer dielectric; and

forming a plate line (87) that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors.

Regarding claim **21**, Kim et al. disclose in Fig. 5 the method further comprises:

forming hydrogen barrier spacers (83a) between sidewalls of the ferroelectric capacitors and the lower interlayer dielectric; and

forming an upper interlayer dielectric (89) on the lower interlayer dielectric and the plurality of ferroelectric capacitors.

Regarding claim **23**, Kim et al. disclose in Fig. 5 the method wherein the forming a plate line comprises forming the plate line on sidewalls of the hydrogen barrier spacers and a surface of the lower interlayer dielectric.

Regarding claim **24**, Kim et al. disclose in Fig. 26 the method wherein forming the plate line comprises:

forming a lower plate layer (PP) on the semiconductor substrate and the hydrogen barrier spacers; and

pattering the lower plate layer to form a plurality of parallel local plate lines,

wherein each of the local plate lines directly contacts surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors.

Regarding claim **25**, Kim et al. disclose in Figs. 11, 12 and 26 the method wherein prior to the forming the lower plate line, the method further comprises:

forming an insulation layer (85) on the semiconductor substrate and the hydrogen barrier spacers; and

planarizing the insulation layer until surfaces of the ferroelectric capacitors are exposed, and leaving an insulation pattern (85a) filling a gap region between the ferroelectric capacitors.

Regarding claim **26**, Kim et al. disclose in Fig. 26 the method wherein after forming the local plate line, the method further comprises sequentially forming a first upper interlayer dielectric layer (89) and a second upper interlayer dielectric layer (93) on the local plate lines.

Regarding claim **27**, Kim et al. disclose in Fig. 26 the method further comprises:

successively patterning the second and first interlayer dielectric layers to form a slit-type via hole (95c) exposing a portion the local plate lines; and

forming a main plate line (97) covering the slit-type via hole.

Regarding claim **28**, Kim et al. disclose in Fig. 26 the method wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer (77), a ferroelectric layer (79), and an upper electrode layer (81) on the lower interlayer dielectric; and

successively patterning the upper electrode layer, the ferroelectric layer, and the lower electrode layer to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures (82) that are arranged in row and column directions.

Regarding claim **29**, Kim et al. disclose in Fig. 26 the method wherein sidewalls of the ferroelectric capacitors have an inclination of about 70° to about 90°.

Regarding claim **34**, Kim et al. disclose in Figs. 11 and 26 the method wherein the forming the hydrogen barrier spacers comprises:

conformally forming a hydrogen barrier layer (83) on the ferroelectric capacitors and the semiconductor substrate; and

anisotropically etching the hydrogen barrier layer until surfaces of the ferroelectric capacitors are exposed,

wherein the hydrogen barrier layer is formed from at least one material selected from the group consisting of TiO_2, Al_2O_3, ZrO_2, and CeO_2 (see [0026]).

Regarding claim **35**, Kim et al. disclose in Figs. 12, 13 and 26 the method wherein forming the upper interlayer dielectric and the forming the plate line comprises:

sequentially forming first and second upper interlayer dielectrics (89, 93) on the hydrogen barrier spacers (85a) and the semiconductor substrate; and

successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole (95) exposing a surface of the ferroelectric capacitor in a row direction; and

forming a main plate line (97) covering the slit-type via hole.

Regarding claim **36**, Kim et al. disclose in Figs. 12, 13 and 26 the method wherein the slit-type via hole exposes a surface of the lower interlayer dielectric between the ferroelectric capacitors.

Regarding claim **37**, Kim et al. disclose in Figs. 12, 13 and 26 the method wherein the forming the slit-type via hole comprises leaving a portion of the first upper interlayer dielectric between the hydrogen barrier spacers.

Regarding claim **38**, Kim et al. disclose in Figs. 12, 13 and 26 the method wherein the sequentially forming first and second upper interlayer dielectrics comprises forming main word lines between the first and second upper interlayer dielectrics.

Allowable Subject Matter

Claims **8, 9, 11, 12 and 30-33** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

09/24/04

Andy Huynh

Patent Examiner